E-COMMERCE SECURITY PROCESSOR ALIGNMENT LOGIC

ABSTRACT

Provided is an architecture for a cryptography accelerator chip that allows significant performance improvements over previous prior art designs. The chip architecture enables a degree of parallel processing of authentication and encryption/decryption functions achieved by an alignment logic configuration that distinguishes portions of a non-pre-padded network security protocol (e.g., SSL (v3) or TLS) packet requiring one and/or another operation (authentication and/or encryption) to permit single pass processing of non-pre-padded network security protocol data. In some embodiments, processing efficiency may be further enhanced by the pipelining of successive packets to be processed.